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The DDR Subsystem (DDRSS) Is Composed Of 2 Main Parts: • The DDR Controller (DDCTRL) • The DDR PHY (DDRPHYC) DFI Is The Standard Interface Between The DDR Controller And The DDR PHY The DDRCTRL Is In Charge Of: • Convert AXI Bus Transactions To DRAM Transfers At DFI Interface • AXI Feb 1th, 2024

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Into The Line 1 Jacks Of The Light/Amp Box (which We Will Call The LA From Now On), And The Other End Into Our Laptop's Headphone Jack. Viewed From The Rear, The LAB Is The Metal Box And The JPAC Is Mounted Below, With The JAMMA Harness Plugged Into Jan 25th, 2024

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