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Redis In Action. Manning Publications Co., 2013. [4] Dhruva R Chakrabarti, Hans-J Boehm, And Kumud Bhandari. Atlas: Leveraging Locks For Non-volatile Memory Consistency. ACM SIGPLAN Notices, 49(10):433–452, 2014. [5] Himanshu Chauhan, Irina Calciu, Vijay Chidambaram, Eric Schkufza, Feb 1th, 2024

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Chapter 8 Memory Hierarchy And Cache Memory

• Suppose Processor Has 2 Levels Of Hierarchy: Cache And Main Memory • T Cache = 1 Cycle, T MM = 100 Cycles • What Is The AMAT Of The Program From Example 1? AMAT = T Cache + MR Cache (t MM) = [1 + 0.375(100)] Cycles = 38.5 Cycles Memory Performance Example 2 Jan 22th, 2024

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