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VHDL Code And Implemented With The Targeted Device XC3S500E. The Multiplier Is Designed For 8-bit Wide Operands. The Addition Operation Is Done By Using Parallel

Prefix Adder (16-bit). The Performance Of Multiplier Block Is Tested For Various Parallel Prefix Adder Variants Such As BK, Sklansky, KS, HC, LF, Mar 6th, 2024

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