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System Architecture For Multi-Technology Testbench-on-a-Chip Angela Hodge<sup>1,2</sup>, Robert Newcomb<sup>2</sup>, Mona Zaghoul<sup>3</sup>, And Onur Tigli<sup>3</sup> <sup>1</sup>Naval Research Laboratory <sup>2</sup>University Of Maryland At College Park <sup>3</sup>The George Washington University 4555 Overlook Avenue, S.W. Department Of Electrical Engineering Department Of Electrical And Computer Engineering Apr 13th, 2024

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6. John Aynsley, "Easier UVM For Functional Verification By Mainstream Users", DVcon, Mar-2011 7. Martin Keaveney, Anthony McMahon, Niall O'Keeffe, Kevin Keane, James O'Reilly, "THE DEVELOPMENT OF ADVANCED N ENVIRONMENTS USING SYSTEM VERILOG", ISSC(International System Safety Conference), June-2008 8. Jan 2th, 2024

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