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Is Shown Below. There Are Two States Defined Based
On Carry. The State S 0 Is For Carry Equal To Zero And
S 1 Is For Carry ... 6th, 2024Figure 6.30.

Implementation Of The FSM Of Figure 6.3 In A ...Figure
6.49. Verilog Code For The Serial Adder. Module
Serial_adder (A, B, Reset, Clock, Sum); Input [7:0] A, B;
Input Reset, Clock; Output Wire [7:0] Sum; 3th, 2024.
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